Amendments to the Claims

This listing of claims will replace all prior versions and listing of claims in the application:

1. (Previously Presented) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate and including a plurality of gate lines and a plurality of gate electrodes;

a storage electrode wire formed on the insulating substrate and including a plurality of storage electrode lines and a plurality of storage electrodes;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the gate insulating layer and including a plurality of data lines insulated from and crossing over the gate lines, a plurality of source electrodes contacting the semiconductor layer at least in part, a plurality of drain electrodes facing the source electrodes and contacting the semiconductor layer at least in part;

a passivation layer formed on the data wire;

a plurality of pixel electrodes formed on the passivation layer and electrically connected to the drain electrodes;

an active area for displaying images and comprising the plurality of pixel electrodes, a portion of the gate wire, a portion of the storage wire and a portion of the data wire;

a peripheral area surrounding the active area;

a first common bar electrically connected to a plurality of storage wire and formed in a first portion of the peripheral area; and

a second common bar electrically connected to the plurality of stroage wire and formed in a second portion of the peripheral area,

wherein the widths of the first and second common bars are different, and the first and second portions of the peripheral areas are on opposite sides of the active area.

2. (Previously Presented) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate and including a plurality of gate lines and, a plurality of gate electrodes;

a storage electrode wire formed on the insulating substrate and including a plurality of storage electrode lines and a plurality of storage electrodes;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the gate insulating layer and having a triple-layered structure including an amorphous silicon layer, an ohmic contact layer, and a metal layer, the data wire including a plurality of data lines, a plurality of source electrodes connected to the data lines, and a plurality of drain electrodes facing the source electrodes;

a passivation layer formed on the data wire;

a plurality of pixel electrodes formed on the passivation layer and electrically connected to the drain electrodes;

an active area for displaying images and comprising the plurality of pixel electrodes, a portion of the gate wire, a portion of the storage wire and a portion of the data wire;

a peripheral area surrounding the active area;

a first common bar electrically connected to a plurality of storage wires and formed in a first portion of the peripheral area; and

a second common bar electrically connected to the plurality of stroage wires and formed in a second portion of the peripheral area,

wherein the widths of the first and second common bars are different, and the first and second portions of the peripheral areas are on opposite sides of the active area.

3. (Canceled)

4. (Canceled)

5. (Previously Presented) A thin film transistor array panel comprising:

an insulating substrate;

a plurality of first signal lines formed on the insulating substrate and extending in a first direction;

a plurality of second signal lines formed on the insulating substrate and extending in the first direction;

a third signal line insulated from and crossing the first and second signal lines and

extending in a second direction;

a plurality of pixel electrodes formed on the substrate;

a plurality of thin film transistors connected to the first signal lines, the third signal lines, and the pixel electrodes;

an active area for displaying images and comprising the plurality of pixel electrodes, a portion of the plurality of first signal lines, a portion of the plurality of second signal lines and a portion of the plurality of the third signal lines;

a peripheral area surrounding the active area;

a first common bar electrically connected to the plurality of the second signal lines and formed in a first portion of the peripheral area; and

a second common bar electrically connected to the plurality of the second signal lines and formed in a second portion of the peripheral area,

wherein the widths of the first and second common bars are different, and the first and second portions of the peripheral areas are on opposite sides of the active area.

6. (Canceled)

7. (Currently Amended) A thin film transistor array panel comprising:

an insulating substrate;

a plurality of first signal lines formed on the insulating substrate and extending in a transverse direction, and including a plurality of first signal pads;

a plurality of second signal lines formed on the insulating substrate and extending in a transverse direction;

a plurality of third signal lines insulated from and intersecting the first and the second signal lines and extending in a longitudinal direction;

a plurality of pixel electrodes formed on the substrate;

a first common bar connecting ends of the second signal lines located opposite the first signal pads; and

a second common bar connecting ends of the second signal lines located near the first signal pads,

wherein the second ~~the~~ common bar has a width equal to or less than 150 microns, the widths of the first and second common bars are different, and the first and the second common bars are

formed in a peripheral area surrounding an active area comprising a plurality of thin film transistors.

8. (Canceled)

9. (Previously Presented) The thin film transistor array panel of claim 1, wherein the storage electrode wire is formed simultaneously with the gate wire; and

wherein a first group of storage electrode lines are formed parallel to the gate lines and a second group of storage electrode lines are formed perpendicular to the gate lines.

10. (Canceled)

11. (Canceled)

12. (Previously Presented) The thin film transistor array panel of claim 2, wherein the storage electrode wire is formed simultaneously with the gate wire; and

wherein a first group of storage electrode lines are formed parallel to the gate lines and a second group of storage electrode lines are formed perpendicular to the gate lines.

13. (Canceled)

14. (Previously Presented The thin film transistor array panel of claim 5, wherein a first portion of the plurality of second signal lines extends in transverse direction and a second portion of the plurality of second signal lines extends in longitudinal direction in the active area.

15. (Canceled)

16. (Previously Presented) The thin film transistor array panel of claim 7, wherein a first portion of the plurality of second signal lines extends in transverse direction and a second portion of the plurality of second signal lines extends in longitudinal direction in the pixel areas.

17. (Currently Amended) The thin film transistor array panel of claim 1, further comprising a ~~purality~~ plurality of gate pads in the first portion of the peripheral area, wherein the width of the first common bar is smaller than the width of the second common bar.

18. (Previously Presented) The thin film transistor array panel of claim 2, further comprising a plurality of gate pads in the first portion of the peripheral area, wherein the width of the first common bar is smaller than the width of the second common bar.

19. (Previously Presented) The thin film transistor array panel of claim 5 further comprising a plurality of second pads in the first portion of the peripheral area, wherein the width of the first common bar is smaller than the width of the second common bar.

20. (Previously Presented) The thin film transistor array panel of claim 7 further comprising a plurality of second pads in the first portion of the peripheral area, wherein the width of the first common bar is smaller than the width of the second common bar.